

**AMENDMENTS TO THE ABSTRACT**

Please substitute the following paragraph(s) for the abstract now appearing in the currently filed specification:

**ABSTRACT OF THE DISCLOSURE**

A shift register includes unit circuits cascade-connected to form a plurality of shift stages. Each of the unit circuits has a time-shifter including a NAND circuit to receive an input pulse as one input thereof, and a holder having a PMOS transistor and a NMOS transistor, ~~which are~~ connected in series between a power supply and a clock input ~~end fed with a clock pulse and of~~ which gates and drains are mutually connected in common respectively. The input ~~end of~~ the holder is connected to the output ~~end of~~ the NAND circuit, and the output ~~potential~~ thereof is fed as another input to the NAND circuit. The odd-stage unit circuits and the even-stage unit circuits operate in synchronism respectively with clock pulses having a 1/4 phase difference from each other. ~~The holder holds the shifted pulse synchronously with the clock pulse, and then outputs the shifted pulse.~~ In this structure, the number of transistors between the positive and negative power supplies can be reduced for lowering the required supply voltage and accelerating the shift register operation.